



**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**FEB 05 2002**

**Technology Center 2600**

**In re Application of:**

Leonard Forbes

**Serial No.:** 09/943,968

**Filed:** August 30, 2001

**For:** TECHNIQUE TO SIMULTANEOUSLY  
DISTRIBUTE CLOCK SIGNALS AND DATA  
ON INTEGRATED CIRCUITS,  
INTERPOSERS, AND CIRCUIT BOARDS

**Examiner:** Unknown

**Group Art Unit:** 2631

**Attorney Docket No.:** 4720US (00-1120)

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail (under 37 C.F.R. § 1.8(a)) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

January 10, 2002  
Date of Deposit

*Darlene Holt*  
Signature of registered practitioner or other person  
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1.8(a)(1)(ii)

Darlene Holt  
Typed/printed name of person whose signature is  
contained above

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56(b) exists.

DOCUMENTS

Other Documents

K. Yip, "Clock tree distribution: balance is essential for a deep-submicron ASIC design to flourish," IEEE Potentials, Vol. 16, no. 2, pp 11-14, April-May 1997.

K. M. Carrig et al., "A Clock methodology for high-performance microprocessors," Proc. Custom Integrated Circuits Conference, Santa Clara, CA, May 5-8, pp. 119-122, 1997.

J. L. Neves et al., "Automated synthesis of skew-based clock distribution networks," VLSI Design, Vol. 7, no.1, pp. 31-57, 1998.

T. Meincke et al., "Globally asynchronous locally synchronous architecture for large high-performance ASICs," IEEE Symp. on Circuits and Systems, Orlando, FL, 30 May-2 June, Vol. 2, pp. 512-515, 1999.

Applicant offers to supply any explanation or discussion of the documents that the Examiner feels is necessary or desirable and which is requested.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: January 10, 2002

DRJ/hlg:dh

Enclosures: Form PTO-1449

Copy of documents cited

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